

ENCQOR 5G SME/Academic Technology Development Challenge

A Comprehensive Clock Synchronization Solution for 5G Networks using IEEE 1588v2 Protocol

Challenge Launch Date	<ul style="list-style-type: none"> April 4, 2019
Challenge Deadline	<ul style="list-style-type: none"> May 2, 2019
Challenge Statement	<p>A Comprehensive Clock Synchronization Solution for 5G Networks using IEEE 1588v2 Protocol</p> <p>5G networks have stringent requirements for frequency and time synchronization and the relevant standards are under study. 5G packet-based networks could be used to meet these requirements, however, accuracy between the master and slave clocks may suffer due to many factors. Ciena is interested in developing a clock model derived from the IEEE 1588v2 PTP master-slave message exchange to measure the correct offset value in a slave clock in the presence of different network conditions use cases and asymmetric latencies. Ciena is also interested in developing a mathematical and forecasting model to train the clock model to compensate temperature and aging effects on the slave clock rate.</p>
Project Partner	Ciena Corporation
Timeline	2 years
Available funding	<ul style="list-style-type: none"> up to \$150,000
<ul style="list-style-type: none"> Applicant Type 	<ul style="list-style-type: none"> Ontario based College/University
<ul style="list-style-type: none"> Location 	<ul style="list-style-type: none"> Applicant could use two interconnected network elements, and best applied to a multiple hop network in the ENCQOR network Infrastructure. Applicant could also execute part of the work at their own facility/institution as required. Applicant might need to meet people at Ciena on occasion.
Project Details	<p>Next generation 5G mobility networks have stringent requirements for frequency and time synchronization and the relevant standards are under study. As per ITU Telecommunications Standardization Sector (ITU-T) G.8262.1 standard (draft), 5G NR will require time synchronization between 390 ns (basic) and 130 ns (high-level). To meet these requirements, IEEE 1588v2 PTP is an excellent candidate for 5G packet-based networks. However, IEEE 1588v2 PTP synchronization accuracy between master and slave clocks can be affected by several factors including:</p> <ul style="list-style-type: none"> Asymmetric latency can be caused by packet delay variation (PDV) or delay jitter in timing packets that deteriorates the synchronization accuracy severely. In addition, tx/rx fiber

asymmetry, changes in network topology, routing path reconfiguration, traffic loads, temporary network outages defined in ITU-T standards further aggravate the asymmetric latency problem.

- The equipment needed to translate between communication protocols in the network can be a source of impairments that affects clock synchronization accuracy.
- Clock rate/drift due to temperature and aging effects on the slave clock(s) can affect synchronization accuracy. Clocks are typically made from inexpensive oscillator circuits, or battery backed quartz crystals. Each of these clocks tends to drift due to inherent instabilities in the source of oscillator, in addition to environmental factors such as temperature, aging, manufacturer imprecision, air pressure, mechanical pressure etc.

Considering these challenges, the goal of the project is to develop a clock model derived from the IEEE 1588v2 PTP master-slave message exchange and measure the correct offset value in a slave clock in the presence of different network conditions and asymmetric latencies.

A second project goal is to develop a mathematical and forecasting model to train the clock model to compensate temperature and aging effects on the slave clock rate by computing the correctional rate from the slope of the most recent set of calculated offsets.

The scope of the project work is to develop a comprehensive clock model that meets the following requirements:

- Develop the clock model using the IEEE 1588v2 synchronization protocol, measure clock offset and update slave clock considering different network changes, uses cases, asymmetric traffic conditions and PDV defined in ITU-T standards (8261.1, G.8262.1, G.8273.2, 8275.1, 8275.2) for 5G network.
- Introduce to support multiple master clocks instead of selecting a grandmaster clock to ensure the slave clock receives at least one good offset sample from one of these master clocks within the defined update frequency interval. 2nd master clock will also act as redundant clock source.
- Develop a multi-stage filtering method to determine a good offset sample derived from the IEEE 1588v2 PTP master-slave message exchange and update the slave clock for maintaining high synchronization accuracy. Alternative technique could be to develop a method so that timing packet can avoid queuing buffers that causes PDV.
- Incorporate a forecasting model (ARIMA/LES) to train the clock model by continuously monitoring the calculated offsets and good offset values and use this to to update the slave clock when it will suffer due to high asymmetric latency.

	<ul style="list-style-type: none"> • Develop a mathematical model to incorporate the temperature and ageing effects on slave clock rate and use the forecasting model to train the clock model to compensate temperature and aging effects on the slave clock rate and improve the accuracy and stability of the slave clock during holdover mode. • The solution should define performance evaluation matrix of the clock model by leveraging different use cases defined in ITU-T documentations (e.g. 8261.1, G.8262.1, G.8273.2, 8275.1, 8275.2) defined for 5G network and use ENCQOR network infrastructure as test bed.
<p>Project Goals/ Outcomes</p>	<p>Project Outcomes:</p> <ul style="list-style-type: none"> • The development and delivery of the clock model with the functionality described in the Project Details Section • The development and delivery of the mathematical forecasting model for slave clock offset. <p>ENCQOR Outcomes: With the use of Carrier Ethernet Network (CEN) for backhaul and, potentially, for fronthaul and midhaul in the future it creates an opportunity to implementan IEEE 1588v2 timing distribution solution on the ENCQOR network. This could be done using a dedicated Class of Service (CoS) or a dedicated virtual circuit (VC) with stringent requirements on Frame Loss Ratio, Frame Delay and Inter-Frame Delay Variation to minimize performance impairments on network synchronization of 5G NRs.</p> <p>Upon incorporating this clock model within Ciena equipment, it would open the opportunity to expand Ciena’s role within the ENCQOR fronthaul and midhaul network.</p>
<p>Applicant Capabilities</p>	<p>The applicant should have solid background knowledge and experience in:</p> <ul style="list-style-type: none"> • mathematics • software programming • networking
<p>Additional Information</p>	<p>References or external sources of information:</p> <ul style="list-style-type: none"> • ITU-T Profiles- 8261.1, G.8262.1, G.8273.2, 8275.1, 8275.2. [Online], available: https://www.itu.int/rec/ • Aamir Mahmood, Muhammad Ikram Ashraf, Mikael Gidlund, and Johan Torsner, <i>“Over-the-Air Time Synchronization for URLLC: Requirements, Challenges and Possible Enablers”</i>, 2018 15th International Symposium on Wireless Communication Systems (ISWCS) • Daniel Philip Venmani, Yannick Lagadec, Olivier Lemoult, Fabrice Deletre, <i>“Phase and Time Synchronization for 5G C-RAN: Requirements, Design Challenges and Recent Advances in Standardization”</i>, EAI Endorsed Transactions on Industrial Networks

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Launched in 2018, the [ENCQOR 5G SME Technology Development Program](#) Partners Ontario based SMEs with ENCQOR 5G Anchor Firms on 5G technology development projects. Areas of research interest are defined by Challenge Statements submitted to OCE by the [ENCQOR 5G Anchor Firms](#) and posted to the [OCE website on a rolling basis](#).

If you are interested in developing an expression of interest, please visit the [program guidelines](#) for information on next steps.

For any questions about new Challenge Statements or the ENCQOR 5G SME Technology Development Program please contact Sarah Fairlie at sarah.fairlie@oce-ontario.org