ENCQOR 5G Technology Development Challenge

Custom ASIC for at-speed test of Optical signal path

Challenge Launch Date	October 10, 2019
Challenge Deadline	November 7, 2019
Challenge Statement	Integrated Circuits used in the optical signal transmit and receive paths require at-speed testing in production. Existing test technology in semiconductor automatic test equipment (ATE) does not support this requirement. Instruments embedded in the test head cannot provide the RF signals required and if they are added as either new instruments or external instruments, the physical length of the signal path renders them unusable due to noisy interference and uncontrolled parasitic impedance. Custom Integrated Circuits (IC) that can generate or receive the required signals and can be embedded on a probe card very close to the device being tested are required to solve this challenge.
Project Partner	Ciena
Timeline	12 months
Available funding	Up to $500,000 CDN
Applicant Type	Ontario SME with expertise in mixed-signal IC development and IC manufacturing test.
Location	Most of the design work can be completed remotely. Some visits to Ciena (Ottawa) may be needed for design and requirements reviews.
Project Details	Advanced optical networking equipment used in 5G networks employ advanced signal processing techniques to communicate data over long distances. Testing of highly integrated A/D and D/A conversion at the front-end of high-speed optical transceivers is ever more challenging. In recent IC development, circuitry has been included as a built-in self-test function in the transceiver to support manufacturing test with stimulus generation to drive test signals and monitoring functions. These circuits are becoming prohibitively difficult to include in new designs as power and area budgets are becoming more constrained. The newest transceiver designs support interface aggregate data rates of over 800 Gbps with individual channels operating at carrier frequency of over 25 GHz. Moving forward, testing of these designs must be executed with an automatic external test function however the physical limitations of external test equipment remain a challenge for these systems. The long distance between test equipment and the device under test preclude the use of commercial test instruments because of the signal distortion incurred in the long wires, signal traces, and discontinuities at connectors.

	The challenge is to develop an external test solution that delivers the same driver and monitoring functions as the internal test hooks developed for older generations of the technology as described above. This solution must be implemented on the ATE load board in the manufacturing test environment. It must also provide similar or better test capability than the existing built-in self-test solution. The solution must overcome the challenge of additional signal distortion imparted by interference and parasitic impedance caused by the longer distance and material interfaces between the test circuits and the device under test. The solution must include the external IC design for the driver and monitor functions. It must also include a method for integrating the monitor and driver functions into the transceiver manufacturing test program. It must support ATE-compatible signaling protocols for real-time communications (up to 10 Mbps) between the solution and the test program. Ciena will work with the successful SME applicant to: • Integrate proprietary Ciena driver and monitor functions into external ICs. • Create a method for integrating these functions into existing test solutions. • Examine the performance of the external interface and load board to make recommendations to design requirements.
Project Goals/ Outcomes	Ciena is interested in developing prototype ICs that can be integrated directly into ATE load boards and communicate directly with ATE software for further test development. The driver and monitor should be delivered separately as two discrete ICs to facilitate load board PCB design and for best electrical performance. The IC deliverable must also include methods for communicating with the external driver and monitor through ATE software without the need for additional hardware or software.
Applicant Capabilities	• Mixed-signal IC design knowledge of A/D and D/A data converters • IC design IT and EDA infrastructure • Expertise in manufacturing test development for high-speed A/D and D/A converters. • Semiconductor ATE software development
Additional Information	Work in co-operation with Ciena's transceiver IC and test development teams to develop a prototype test system.

Launched in 2018, the ENCQOR 5G SME Technology Development Program partners Ontario based SMEs with ENCQOR 5G Anchor Firms on 5G technology development projects. Areas of research interest are defined by Challenge Statements submitted to OCE by the ENCQOR 5G Anchor Firms and posted to the OCE website on a rolling basis.

If you are interested in developing an expression of interest, please visit the program guidelines for information on next steps.

For any questions about new Challenge Statements or the ENCQOR 5G SME Technology Development Program please contact Jennifer Moles at Jennifer.Moles@oce-ontario.org.